

WHAT IS CLAIMED IS:

1. A delay lock loop circuit comprising:

a dividing means for generating, on a clock signal, first pulse data, second pulse data having a period greater than that of said first pulse data, and third pulse data having a period greater than that of said second pulse data;

an up/down counter having a sub counter, to a count value of which an initial value, a maximum value, and a minimum value are set, said sub counter executing at least one of a count-up operation and a count-down operation on the basis of up/down control signal at a rising edge of said third pulse data and, when said count value has reached said maximum value and said minimum value, setting a next count value to said initial value, said up/down counter executing a count-up operation at a rising edge of said third pulse data when said count value of said sub counter is said maximum value and a count-down operation when said count value is said minimum value;

a delay means for delaying said first pulse data in accordance with the number of delay steps based on a count output of said up/down counter;

a delay amount detecting means for determining

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which of a rising edge of said second pulse data and a rising edge of an output pulse of said delay means comes first and outputting, on the basis of a result of this determination, said up/down control signal; and

a delay lock detecting means for comparing a current count value with a past count value of said up/down counter at a rising edge of said third pulse data to determine whether or not a delay amount is locked, selecting one of said current count value and said past count value, and outputting the selected count value as a reference delay step count.

2. The delay lock loop circuit according to claim 1, wherein said sub counter comprising:

a latch means for latching supplied data at a rising edge of said third pulse data;

an adding means for adding 1 to a latch data value supplied from said latch means;

a subtracting means for subtracting 1 from said latch data value;

a first comparing means for, if said latch data value is equal to said maximum value, outputting a first reset signal indicative thereof;

a second comparing means for, if said latch data value is equal to said minimum value, outputting a second

reset signal indicative thereof;

a first selector for selectively outputting, on the basis of said up/down control signal, data supplied from said adding means and said subtracting means; and

a second selector supplying, to said latch means, said initial value if one of said first reset signal and said second reset signal is supplied and the output data of said first selector in any other cases.

3. A variable delay circuit comprising:

a reference delay step count output means having

a dividing means for generating, on a clock signal, first pulse data, second pulse data having a period greater than that of said first pulse data, and third pulse data having a period greater than that of said second pulse data,

an up/down counter having a sub counter, to a count value of which an initial value, a maximum value, and a minimum value are set, said sub counter executing at least one of a count-up operation and a count-down operation on the basis of up/down control signal at a rising edge of said third pulse data and, when said count value has reached said maximum value and said minimum value, setting a next count value to said initial value, said up/down counter executing a count-up operation at a

rising edge of said third pulse data when said count value of said sub counter is said maximum value and a count-down operation when said count value is said minimum value,

a first delay means for delaying said first pulse data in accordance with the number of delay steps based on a count output of said up/down counter,

a delay amount detecting means for determining which of a rising edge of said second pulse data and a rising edge of an output pulse of said first delay means comes first and outputting, on the basis of a result of this determination, said up/down control signal, and

a delay lock detecting means for comparing a current count value with a past count value of said up/down counter at a rising edge of said third pulse data to determine whether or not a delay amount is locked, selecting one of said current count value and said past count value, and outputting the selected count value as a reference delay step count;

a delay step count setting means, to which said clock signal is supplied, for multiplying said reference delay step count with a delay rate; and

a second delay means, configured in substantially a same manner as said first delay means, for delaying

inputted data on the basis of a delay step count set by said delay step count setting means.

4. A recording signal compensating circuit for recording data to a disk recording medium in accordance with a recording pulse obtained by synthesizing a leading pulse, a burst pulse, and a trailing pulse, comprising:

a reference delay step count output means having a dividing means for generating, on a clock signal, first pulse data, second pulse data having a period greater than that of said first pulse data, and third pulse data having a period greater than that of said second pulse data,

an up/down counter having a sub counter, to a count value of which an initial value, a maximum value, and a minimum value are set, said sub counter executing at least one of a count-up operation and a count-down operation on the basis of up/down control signal at a rising edge of said third pulse data and, when said count value has reached said maximum value and said minimum value, setting a next count value to said initial value, said up/down counter executing a count-up operation at a rising edge of said third pulse data when said count value of said sub counter is said maximum value and a count-down operation when said count value is said

minimum value,

a first delay means for delaying said first pulse data in accordance with the number of delay steps based on a count output of said up/down counter,

a delay amount detecting means for determining which of a rising edge of said second pulse data and a rising edge of an output pulse of said first delay means comes first and outputting, on the basis of a result of this determination, said up/down control signal, and

a delay lock detecting means for comparing a current count value with a past count value of said up/down counter at a rising edge of said third pulse data to determine whether or not a delay amount is locked, selecting one of said current count value and said past count value, and outputting the selected count value as a reference delay step count;

a delay step count setting means to which said clock signal is supplied, for multiplying said reference delay step count with a delay rate;

a second delay means, configured in substantially a same manner as said first delay means, for delaying inputted data on the basis of a delay step count set by said delay step count setting means;

a leading pulse varying means for varying a pulse

width of said leading pulse by delaying a leading edge position of said leading pulse; and

a trailing pulse varying means for varying a pulse width of said trailing pulse by delaying a trailing edge position of said trailing pulse.

5. A delay lock loop circuit comprising:

a dividing means for generating, on a clock signal, first pulse data, second pulse data having a period greater than that of said first pulse data, and third pulse data having a period greater than that of said second pulse data;

an up/down counter having

a first counter for executing a count-up operation at a rising edge of said third pulse data and, if a count value has exceeded a preset value M (an integer higher than 0), outputting a reset signal and resetting said count value,

a second counter for executing a count-up operation only when an up/down control signal is logically high at a rising edge of said third pulse data and resetting a count value when said reset signal is inputted, and

a third counter for executing a count-up operation only when said up/down control signal is logically low at a rising edge of said third pulse data and resetting a

count value when said reset signal is inputted,

said up/down counter executes, when said reset signal is inputted, a count/up operation if the count value obtained by said second counter is higher than preset value N (an integer higher than 0 and lower than M) and a count-down operation if the count value obtained by said third counter is higher than said preset value N;

a delay means for delaying said first pulse data in accordance with the number of delay steps based on a count output of said up/down counter;

a delay amount detecting means for determining which of a rising edge of said second pulse data and a rising edge of an output pulse of said delay means comes first and outputting, on the basis of a result of this determination, said up/down control signal; and

a delay lock detecting means for comparing a current count value with a past count value of said up/down counter at a rising edge of said third pulse data to determine whether or not a delay amount is locked, selecting one of said current count value and said past count value, and outputting the selected count value as a reference delay step count.

6. The delay lock loop circuit according to claim 5, wherein said up/down counter comprising:

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a first comparing means for, if the count value obtained by said second counter is higher than said preset value N, turning logically high a first flag signal to be outputted;

a second comparing means for, if the count value obtained by said third counter is higher than said preset value N, turning logically high a second flag signal to be outputted; and

a fourth counter for, if said first flag signal is logically high when said reset signal is inputted, executing a count-up operation at a rising edge of said third pulse data and, if said second flag signal is logically high, executing a count-down operation at the rising edge of said third pulse data.

7. A variable delay circuit comprising:

a reference delay step count outputting means having

a dividing means for generating, on a clock signal, first pulse data, second pulse data having a period greater than that of said first pulse data, and third pulse data having a period greater than that of said second pulse data,

an up/down counter having

a first counter for executing a count-up operation

at a rising edge of said third pulse data and, if a count value has exceeded a preset value M (an integer higher than 0), outputting a reset signal and resetting said count value,

a second counter for executing a count-up operation only when an up/down control signal is logically high at a rising edge of said third pulse data and resetting a count value when said reset signal is inputted, and

a third counter for executing a count-up operation only when said up/down control signal is logically low at a rising edge of said third pulse data and resetting a count value when said reset signal is inputted,

said up/down counter executes, when said reset signal is inputted, a count/up operation if the count value obtained by said second counter is higher than preset value N (an integer higher than 0 and lower than M) and a count-down operation if the count value obtained by said third counter is higher than said preset value N,

a first delay means for delaying said first pulse data in accordance with the number of delay steps based on a count output of said up/down counter,

a delay amount detecting means for determining which of a rising edge of said second pulse data and a rising edge of an output pulse of said first delay means

comes first and outputting, on the basis of a result of this determination, said up/down control signal, and

a delay lock detecting means for comparing a current count value with a past count value of said up/down counter at a rising edge of said third pulse data to determine whether or not a delay amount is locked, selecting one of said current count value and said past count value, and outputting the selected count value as a reference delay step count;

a delay step count setting means, to which said clock signal is supplied, for multiplying said reference delay step count with a delay rate; and

a second delay means, configured in substantially a same manner as said first delay means, for delaying inputted data on the basis of a delay step count set by said delay step count setting means.

8. A recording signal compensating circuit for recording data to a disk recording medium in accordance with a recording pulse obtained by synthesizing a leading pulse, a burst pulse, and a trailing pulse, comprising:

a reference delay step count output means having

a dividing means for generating, on a clock signal, first pulse data, second pulse data having a period greater than that of said first pulse data, and third

pulse data having a period greater than that of said second pulse data,

an up/down counter having

a first counter for executing a count-up operation at a rising edge of said third pulse data and, if a count value has exceeded a preset value M (an integer higher than 0), outputting a reset signal and resetting said count value,

a second counter for executing a count-up operation only when an up/down control signal is logically high at a rising edge of said third pulse data and resetting a count value when said reset signal is inputted, and

a third counter for executing a count-up operation only when said up/down control signal is logically low at a rising edge of said third pulse data and resetting a count value when said reset signal is inputted,

said up/down counter executes, when said reset signal is inputted, a count/up operation if the count value obtained by said second counter is higher than preset value N (an integer higher than 0 and lower than M) and a count-down operation if the count value obtained by said third counter is higher than said preset value N,

a first delay means for delaying said first pulse data in accordance with the number of delay steps based

on a count output of said up/down counter,

a delay amount detecting means for determining which of a rising edge of said second pulse data and a rising edge of an output pulse of said first delay means comes first and outputting, on the basis of a result of this determination, said up/down control signal, and

a delay lock detecting means for comparing a current count value with a past count value of said up/down counter at a rising edge of said third pulse data to determine whether or not a delay amount is locked, selecting one of said current count value and said past count value, and outputting the selected count value as a reference delay step count;

a delay step count setting means, to which said clock signal is supplied, for multiplying said reference delay step count with a delay rate;

a second delay means, configured in substantially a same manner as said first delay means, for delaying inputted data on the basis of a delay step count set by said delay step count setting means;

a leading pulse varying means for varying a pulse width of said leading pulse by delaying a leading edge position of said leading pulse; and

a trailing pulse varying means for varying a pulse

width of said trailing pulse by delaying a trailing edge position of said trailing pulse.

9. The recording signal compensating circuit according to claim 4, wherein, let a pulse width for one clock be T and a logically high level and a logically low level of said recording pulse be M and S respectively, then said recording pulse corresponding to a mark of length nT (n being an integer) is represented by one of the following expressions:

$$xS + (1.5-x)M + (n-2)(0.5S + 0.5M) + yM + (0.5-y)S \text{ and}$$

$$xS + (1.5-x)M + (n-3)(0.5S + 0.5M) + 0.5S + yM + (1-y)S.$$

10. The recording signal compensating circuit according to claim 4, further having a burst pulse varying means, configured in substantially a same manner as each of said leading pulse varying means and said trailing pulse varying means, for varying a pulse width of said burst pulse by delaying a position of one of the leading edge and the trailing edge of said burst pulse.

11. The recording signal compensating circuit according to claim 8, wherein, let a pulse width for one clock be T and a logically high level and a logically low level of said recording pulse be M and S respectively, then said recording pulse corresponding to a mark of length nT (n being an integer) is represented by one of

the following expressions:

$$xS + (1.5-x)M + (n-2)(0.5S + 0.5M) + yM + (0.5-y)S \text{ and}$$

$$xS + (1.5-x)M + (n-3)(0.5S + 0.5M) + 0.5S + yM + (1-y)S.$$

12. The recording signal compensating circuit according to claim 8, further having a burst pulse varying means, configured in substantially a same manner as each of said leading pulse varying means and said trailing pulse varying means, for varying a pulse width of said burst pulse by delaying a position of one of the leading edge and the trailing edge of said burst pulse.

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